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Controlling Threshold Voltage of CMOS SOI Nanowire FETs With Sub-1 nm Dipole Layers Formed by Atomic Layer Deposition

Dongqi Zheng, Wonil Chung, Zhizhong Chen, Mengwei Si, Calista Wilk, and Peide D. Ye, *Fellow, IEEE*

***Abstract*—In this article, bidirectional control of threshold voltage (V_T) is realized in both n- and p-silicon-on-insulator (SOI) nanowire FETs (NWFETs) by using sub-1 nm atomic-layer-deposited (ALD) dipole layers (Y_2O_3 and Al_2O_3) for the first time. A 0.7 nm Y_2O_3 inserted between bottom native SiO_x (<1 nm) and top HfO_2 (3 nm) can shift the V_{TH} by −138 and −58 mV for n- and p-NWFET, respectively, while 0.7 nm Al_2O_3 can shift the V_T of n-NWFET by +219 mV and p-NWFET by +134 mV. The tunability of such a high-*k* superstructure for the flat band voltage (V_{FB}) shift of capacitors and V_{TH} shift of planar n-SOI FETs are also investigated. Furthermore, to concisely control the V_{TH} and V_{FB} as design, capacitors fabricated with quadra-layer ($SiO_x/HfO_2/Al_2O_3/Y_2O_3$) high-*k* superstructure were fabricated and 3 mV V_{FB} shift is achieved by carefully adjusting the composition of intermixed-dipole layers. This work points out the route to concisely tune the threshold voltage of complementary metal-oxide-semiconductor (CMOS) FETs with the desired direction and strength.**

***Index Terms*—Atomic layer deposition (ALD), dipole layers, high-*k*, nanowire FET (NWFET), threshold voltage engineering.**

I. Introduction

HIGH-*k* dielectric metal-gate (HKMG) process was first introduced to semiconductor manufacturing in 2007 for high-performance and low-power consumption applications, by reducing the gate leakage current and eliminating polysilicon depletion [1]. However, such progress also brought some new challenges such as the requirement of dual band-edge (DBE) effective work function (EWF) gate metals [2], [3], Fermi-level pinning at the high-*k*/metal interface [4], and undesired threshold voltage shift in the practical applications [5].

Manuscript received October 1, 2021; revised November 26, 2021; accepted December 14, 2021. This work was supported by the Advanced Logic Laboratory at Austin of Samsung Semiconductor, Inc. The review of this article was arranged by Editor L. Ge. *(Corresponding author: Peide D. Ye.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TED.2021.3136493.
Digital Object Identifier 10.1109/TED.2021.3136493

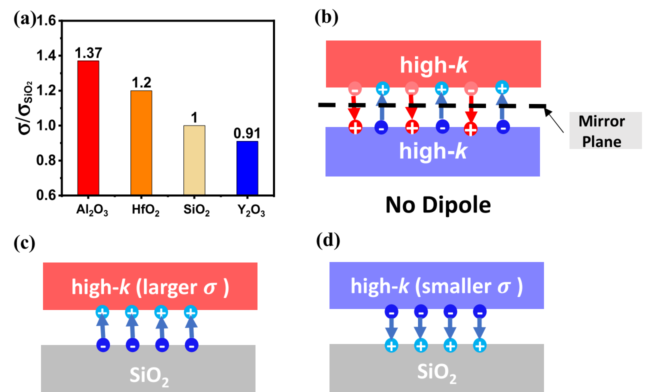

Fig. 1. (a) Normalized oxygen areal density (σ) in different oxides. Schematic of high-*k* dipole formation mechanism between different (b) high-*k* layers, high-*k*/SiO_2 layers with (c) larger and (d) smaller oxygen areal density (σ) compared to SiO_2.

As a result, adjusting the flat-band voltage (V_{FB}) and threshold voltage (V_{TH}) remains a serious challenge that needs to be solved to achieve high-performance high-*k* complementary metal-oxide-semiconductor (CMOS) technologies.

Interface dipole engineering (IDE) is regarded as an effective method to tackle the bottlenecks mentioned above, which is to alter the band alignment by dipole moment formed at the interface of different dielectrics within the MOS stack. Previous work provides both theoretical [6], [7] and experimental evidence [8]–[12] of flat-band voltage shift of high-*k* MOS devices due to the dipole formation at the high-*k*/SiO_2 interface. Among them, the oxygen areal density model proposed by Kita and Toriumi [10] provides a comprehensive explanation for dipole formation mechanisms as well as the V_{FB} shift's dependence on the high-*k* dipole layers. In this model, oxygen ion migration is driven by the diffusion force induced by the difference in the oxygen areal density (σ) between the two oxides. Normalization of different high-*k* oxygen areal densities compared to SiO_2 is concluded in Fig. 1(a), with the order of Al_2O_3 > HfO_2 > SiO_2 > Y_2O_3 [10]. Fig. 1(b)–(d) illustrates that, at the interface, oxygen ions move from a higher-σ layer to a lower-σ layer, leaving vacancies on the

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layer side, and an oxygen ion (with a negative charge) and a vacancy (with a positive charge) is paired to form dipoles. However, at the interface between two high-*k* dielectrics, the movement of both oxygen and metal ions neutralize each other; as a result, no dipoles are formed, which is referred to as the mirror-plane effect. Meanwhile, Fang *et al.* [13] investigate the surface energy-dependent formation of dipole layer at the nonplanar dielectric interface on Si nanowire (NW) by molecular dynamics simulations. The result also shows that built-in potential induced by the surface energy difference on the surface curvature of the dielectric heterointerface plays an important role in the threshold voltage of Si nanowire FETs (NWFETs) or gate-all-around FETs (GAAFETs) [13]. Until now, most of the relevant works in the experiment only focused on the high-*k* dipole layer's tunability of V_{FB} on MOS capacitors and planar transistors. IDE studies on advanced 3-D CMOS structures (fins or NWs) for both n- and p-MOSFET were rarely reported.

In this work, the dipole effects of atomic layer deposition (ALD)-grown Al_2O_3 and Y_2O_3 on HfO_2 are investigated first through high-*k* MOS capacitors and planar MOSFETs. The same gate stacks are successfully integrated into n- and p-type 3-D advanced silicon-on-insulator (SOI) NWFETs and IDE realizes controllable V_{TH} shifts for the first time. Finally, a special design of quadra-layer $SiO_x/HfO_2/Al_2O_3/Y_2O_3$ high-*k* super-structure with compensated dipole effects is proposed and experimentally demonstrated to achieve as small as 3 mV V_{FB} shift in MOS capacitors.

II. Experiments

The fabrication process flow of NW and planar SOI (Si thickness ~70 nm) FETs is shown in Fig. 2(a). Activation of ion-implanted wafers was done in rapid thermal annealing (RTA) chamber at 1000 °C for 60 s. *E*-beam lithography was used throughout the NWFET process. Buried oxide (BOX) under the defined fins was partially selectively etched with HF solution to release the NWs. Dipole layers (Al_2O_3 or Y_2O_3) and the main HfO_2 dielectric (3 nm) were then deposited *in situ* using the same ALD. Trimethylaluminum (TMA), Tris (methylcyclopentadienyl) yttrium, and Tetrakis (dimethyl-amino) hafnium (TDMAH) were used as precursors for the growth of Al_2O_3, Y_2O_3, and HfO_2, respectively, at 250 °C. H_2O was used as an oxidant. Capacitors studied in this work are fabricated on low-doped silicon bulk wafers using the same process as FETs except for channel definition and S/D-related processes. Native SiO_x (<1 nm) was used as an interfacial layer between the high-*k* dielectrics and Si. The gate metal used in this work is fixed as Al. The schematic of the Si NW structure is presented in Fig. 2(b). Fig. 2(c) shows the false-colored SEM images of the side-view (left) and top-view (right) fabricated NW structures immediately after the step of NW release. Multiple parallel ultrathin NWs can be seen as six and ten for the n- and p-NWFET, respectively. An optical image of the planar MOSFET is shown in Fig. 2(d), with the inset image of the gate-stack. High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of the gate-stack is further shown in Fig. 2(e), where the sub-1 nm ALD dipole layer can be

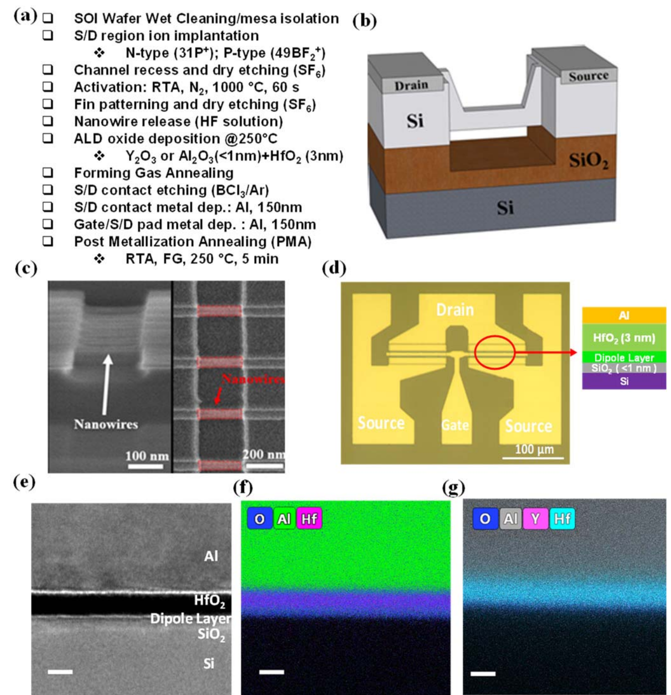

Fig. 2. (a) Process flow of the fabrication of 3-D NWFET (planar devices follow the same process except for steps 3, 5, and 6). (b) Schematic of the NW structure on SOI wafer. (c) SEM image of the 3-D NW SOI structure from side view (left) and top view (right). (d) Optical image of planar FET on SOI with a schematic of high-*k* gate-stack. (e) HAADF-STEM and the corresponding EDS images of the sub-1 nm ALD dipole layer of (f) Al_2O_3 and (g) Y_2O_3 inserted between $HfO_2$and SiO_2, scale bar: 3 nm.

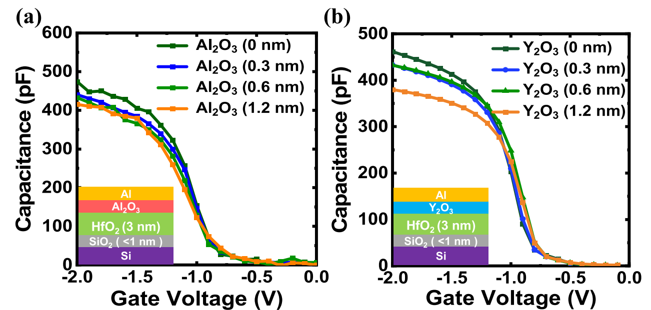

Fig. 3. *C–V* curve of different (a) Al_2O_3 and (b) Y_2O_3 thickness (0–1.2 nm) on top of 3 nm HfO_2 without relative V_{TH} shift observed due to mirror plane formation, with the schematic of dipole layer gate-stack as inset.

observed between HfO_2 and native SiO_x. The dipole layer in this work is referred to as the ultrathin high-*k* layer (Al_2O_3 and Y_2O_3) deposited by ALD to tune the interface dipole properties. Meanwhile, the corresponding EDS images of the sub-1 nm ALD dipole layer of (f) Al_2O_3 and (g) Y_2O_3 inserted between HfO_2 and SiO_x are presented with the scale bar of 3 nm.

III. Results and Discussion

A. Mirror-Plane Effect on Different High-k Interfaces

Mirror-plane phenomena at the interface of Al_2O_3/HfO_2 and Y_2O_3/HfO_2 are first investigated as a reference for the following experiments. *C–V* characteristics are presented in Fig. 3(a) and (b). Different thicknesses ALD dipole layers of

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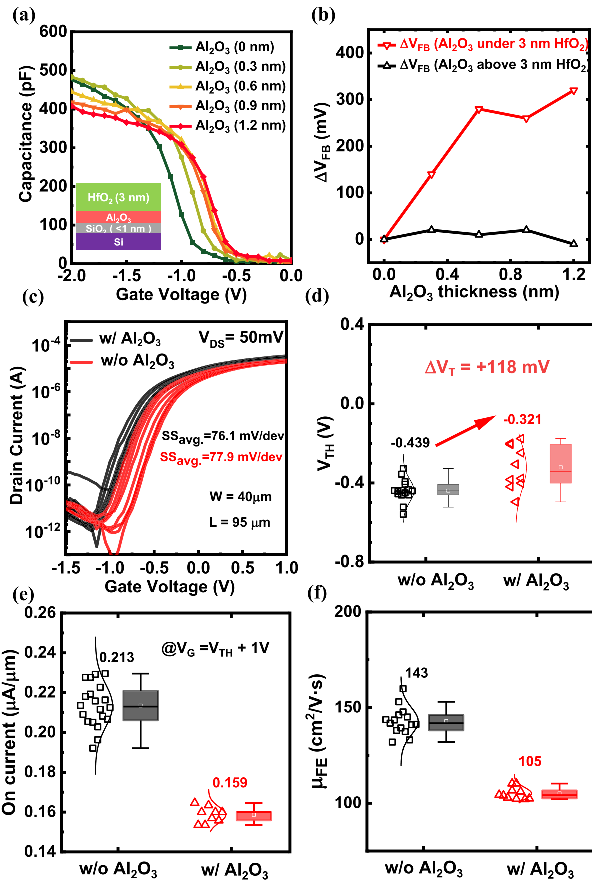

Fig. 4. (a) Schematic of high-k dipole layer stack and C–V curve of different ALD Al_2O_3 thicknesses (0–1.2 nm) under 3 nm HfO_2. (b) Extraction of ΔV_{FB} with Al_2O_3 under or above HfO_2. (c) Statistical transfer curves of n-MOSFET (planar) with 0.56 nm Al_2O_3/3 nm HfO_2 (red) or only 3 nm HfO_2 (black) as the gate-stack, where the channel length is 40 μm and width is 95 μm. (d) Distribution of extracted V_{TH} in two cases with drain current at 0.01 μA/μm and drain voltage at 0.05 V. (e) and (f) Distribution of the ON-current and mobility of the MOSFET with or without Al_2O_3 dipole layer.

Al_2O_3 and Y_2O_3 (from 0 to 1.2 nm) are inserted on top of 3 nm HfO_2. It is noticeable that no V_{TH} shifts are observed in the MOS capacitors as expected, which indicates the movement of oxygen and metal (Hf, Al, Y) ions neutralize each other, therefore, no dipoles are induced.

B. ALD Al_2O_3 Dipole Effect on Capacitors/n-SOI Planar FET

MOS capacitors were first fabricated to preliminarily test the effect of ALD Al_2O_3 dipole layer insertion on V_{FB} (extracted using C–V simulator [14]), Al_2O_3 dipole layers were inserted between SiO_x and HfO_2. The results of the C–V measurement are shown in Fig. 4 in detail. Capacitance is observed to decrease with the increase of equivalent oxide thickness (EOT) and the positive V_{FB} shift is observed when the dipole layer is inserted in direct contact with SiO_x [Fig. 4(a)]. The positive shift is caused by the difference in normalized oxygen areal density of Al_2O_3/SiO_x (+0.37) and HfO_2/SiO_x (+0.2) in the model mentioned above. Such trend can be more clearly observed in Fig. 4(b) where extracted V_{FB} shifted more than +250 mV with Al_2O_3 > 0.6 nm. The ΔV_{FB} gradually saturates when Al_2O_3 thickness (0–1.2 nm) reaches beyond 1 nm, consistent with previous reports [2]. However, as shown in Section III-A, V_{FB} was unaffected when the Al_2O_3 layer was placed on top of 3 nm HfO_2 away from SiO_x, indicating that the dominant interface that shifts V_{FB} is the SiO_x/high-k interface. Planar SOI n-FETs were further fabricated using the same dipole layers to validate the V_{TH} shift trends. Fig. 4(c) shows the transfer curves of all the n-MOSFET devices fabricated with 0.56 nm Al_2O_3/3 nm HfO_2 (red) and only 3 nm HfO_2 (black) as the gate-stack. The subthreshold swings are calculated to be 76.1 and 77.9 mV/dec separately at room temperature, indicating a high-quality interface formed between the channel and oxide stack. Threshold voltages were further extracted in two different gate stacks with drain current fixed at 0.01 μA/μm and drain voltage at 0.05 V. Fig. 4(d) illustrates the distribution of threshold voltages of n-MOSFET with or without Al_2O_3 as the insertion layer, which is −0.321 and −0.439 V, respectively. A positive shift of +118 mV was achieved by employing 0.56 nm ALD Al_2O_3, since the thickness of the Al_2O_3 dipole layer is already ultrathin, the influence of the increase of gate-stack thickness can be neglected in the threshold voltage calculation. Fig. 4(e) and (f) describe the statistical result of the ON-current and mobility of the MOSFETs as fabricated with or without the dipole layer insertion. Mobility is decreased from 143 to 105 cm^2/V·s due to the remote Coulomb scattering (RCS) effect induced by the dipole moments [15]. Meanwhile, ON-current extracted at the gate voltage of V_{TH} + 1 V also drops by around 25% because of the lower mobility and positive threshold voltage shift.

C. ALD Y_2O_3 Dipole Effect on Capacitors and n-SOI Planar FET

A similar process was also carried out to investigate the ALD Y_2O_3 dipole properties. Capacitances of MOS capacitors were first measured in the same way. The Y_2O_3 dipole layers were deposited between SiO_x/HfO_2 and as seen in Fig. 5(a). Like the Al_2O_3case, capacitance is observed to decrease with the thickness increasing, while V_{FB} shifted to the negative direction when the dipole layer inserted in direct contact with SiO_x [Fig. 5(a)]. A larger shift approaching −600 mV can be more clearly observed in Fig. 5(b) with Y_2O_3 > 1.2 nm, with no ΔV_{FB}saturation trend shown. The negative shift can be explained by the difference in normalized oxygen areal density of Y_2O_3/SiO_x (−0.09) and HfO_2/SiO_x (+0.2) in the model mentioned above. Planar SOI n-FETs were further fabricated using the same dipole layers to monitor the threshold voltage shift. The transfer curves of all the n-MOSFET devices fabricated with 0.7 nm Y_2O_3/3 nm HfO_2 (blue) or only 3 nm HfO_2 (black) as the gate-stack are illustrated in Fig. 5(c). The subthreshold swings are measured to be 80.8 and 84.5 mV/dec. Threshold voltages were further extracted, and a shift of −224 mV [Fig. 5(d)] is determined with drain current at 0.01 μA/μm and drain voltage at 0.05 V. Fig. 5(e) and (f) shows the distribution of ON-current and mobility after Y_2O_3 dipole layer insertion, which is rarely investigated in the previous research. As is shown in Fig. 1(a),

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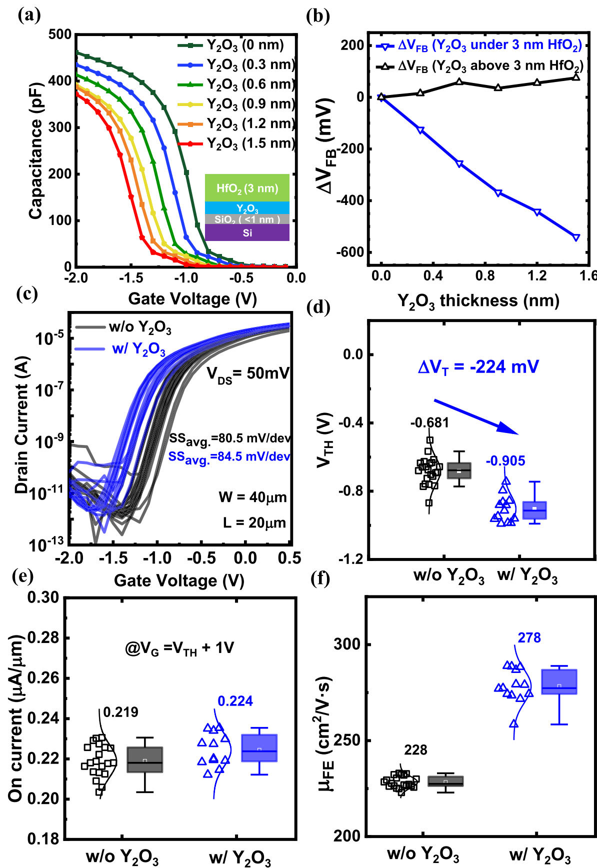

Fig. 5. (a) Schematic of high-*k* dipole layer stack and *C*–*V* curve of different ALD Y_2O_3 thicknesses (0–1.2 nm) under 3 nm HfO_2. (b) Extraction of ΔV_{FB} with Y_2O_3 under or above HfO_2. (c) Statistical transfer curves of n-MOSFET (planar) with 0.7 nm Y_2O_3/3 nm HfO_2 (red) or only 3 nm HfO_2 (black) as the gate-stack, where the channel length is 40 μm and width is 20 μm. (d) Distribution of extracted V_{TH} in two cases with drain current at 0.01 μA/μm and drain voltage at 0.05 V. (e) and (f) Distribution of the ON-current and mobility of the MOSFET with or without Y_2O_3 dipole layer.

the dipole moment formed at the interface of Y_2O_3/SiO_x has an opposite polarity and a weaker strength compared to the reference sample (HfO_2/SiO_x). Under this circumstance, the side effect of RCS induced by the dipole between HfO_2 and SiO_x is eased, thus an increase of mobility can be observed, as well as ON-current due to the higher mobility and negative shift of threshold voltage.

D. ALD Al_2O_3/Y_2O_3 Dipole Effect on 3-D NWFET

Many advanced structures such as FinFET [16], [17], NWFET [18], [19], and GAAFET [20] were proposed to further scale the process node with Moore's law approaching the limit. Among them, the 3-D NW channel is regarded as a promising solution to minimize the short channel effects (SCEs) and improve the device performance at the same time [21]. To address the V_T engineering problem for the state-of-the-art 3-D transistors, sub-1 nm ALD dipole layers were integrated into CMOS NW structures. To place V_T values near 0 V symmetrically for both n- and p-NWFETs, it is critical to be able to shift V_T in both positive and negative

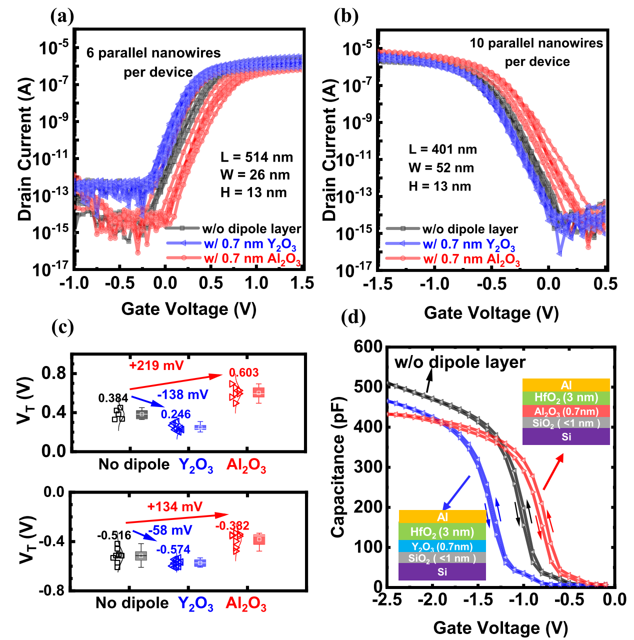

Fig. 6. (a) Overlapped transfer curves of SOI n-NWFETs ($L/W/H$ = 514 nm/26 nm/13 nm) with 0.7 nm of dipole layers (Al_2O_3 or Y_2O_3) under 3 nm HfO_2. (b) Overlapped transfer curves of SOI p-NWFETs ($L/W/H$ = 401 nm/52 nm/13 nm) with 0.7 nm of dipole layers (Al_2O_3 or Y_2O_3) under 3 nm HfO_2. (c) Extracted V_T from **(top)** n-NWFET and **(bottom)** p-NWFET. 0.7 nm of Al_2O_3 and Y_2O_3 dipole layers shift the V_T in positive and negative directions, respectively, for both n- and p-NWFETs. (d) *C*–*V* hysteresis of MOS capacitors fabricated along with SOI n-NWFETs, hysteretic shifts in V_{FB} due to oxide fixed charges are negligible after insertion of dipole layers even with 2.5 V sweep range.

directions with desired strengths. Fig. 6(a) and (b) overlap the transfer curves acquired from multiple SOI n-NWFETs and p-NWFETs with either 0.7 nm of Al_2O_3 (blue circle) or Y_2O_3 (red triangle) grown by ALD method under 3 nm HfO_2. It can be seen from Fig. 6(c) that Y_2O_3 shifted the V_T of both n-NWFETs by −139 mV and p-NWFETs by −58 mV while Al_2O_3 shifted the V_{TH} of n-NWFET by +219 mV and p-NWFET by +134 mV. Shifts in V_{TH} could also be caused by various oxide interface-related trap charges which are usually visible in the form of voltage hysteresis. To evaluate the effect of these charges on V_{TH} shifts, *C*–*V* hysteresis measurements on MOS capacitors fabricated simultaneously with NWFETs were acquired under the sweep voltage larger than 2.5 V, shown in Fig. 6(d). As seen in three *C*–*V* curves, voltage hysteresis caused by interface trap charges are observed to be negligible.

E. Intermixed ALD Al_2O_3/Y_2O_3 Dipole Effect

To further improve the tunability of dipole layers on threshold voltage shift, we introduce the intermixed-dipole engineering, by integrating Al_2O_3 and Y_2O_3into Hf-based high-*k* MOS structure with different compositional ratios. The process flow is shown in Fig. 7(a). Fig. 7(b) illustrates the shift of *C*–*V* curves with Y_2O_3 ALD growth cycles varying from 0 to 2 (0.1 nm/cycle) while Al_2O_3 is fixed at one cycle (0.0875 nm/cycle). Negative V_{FB} shifts of 134 mV (green line, one cycle) and 151 mV (red line, two cycles) are observed

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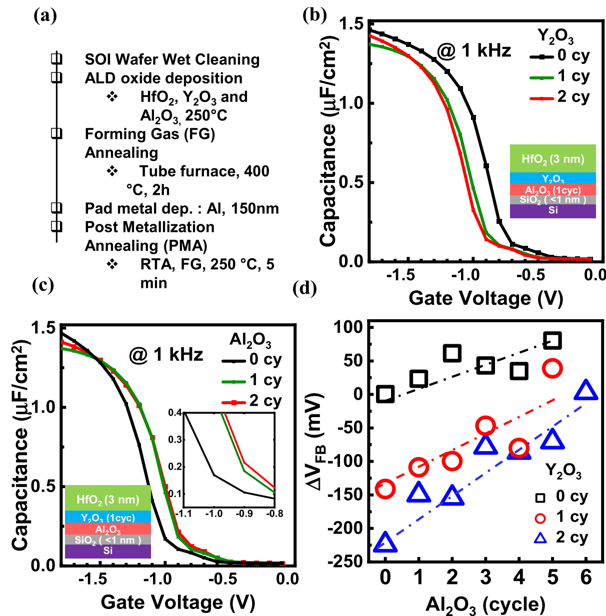

Fig. 7. (a) Fabrication intermixed dipole MOS capacitors. (b) V_{FB} shifts with Y_2O_3 varying from 1 to 3 cycles and Al_2O_3 fixed as one cycle (0.0875 nm/cycle). (c) V_{FB} shifts with Al_2O_3 increasing from 0 to 6 cycles and Y_2O_3 fixed as one cycle (0.1 nm/cycle). (d) V_{FB} shifts with Al_2O_3 increasing from 0 to 6 cycles and Y_2O_3 from 0 to 3 cycles.

compared to the reference sample (without Y_2O_3). Meanwhile, C–V curves of capacitors with Y_2O_3 fixed as one cycle while Al_2O_3 varied from 0 to 2 cycles are described in Fig. 7(c), where $V_{FB}$is positively shifted by 34 and 10 mV, respectively. The V_{FB} shift due to a single Al_2O_3 cycle is relatively weaker than Y_2O_3 in the intermixed dipole system, consistent with the result in the previous section. Furthermore, MOS capacitors with 0–6 cycles Al_2O_3 and 0–3 cycles Y_2O_3 as intermixed dipole layers are fabricated to investigate the turnability of different cases. Fig. 7(d) shows the increasing cycle number of Al_2O_3 and Y_2O_3 can shift the V_{FB} bidirectionally as expected. It is also noticeable that a single Y_2O_3 cycle (without Al_2O_3) can shift V_{FB} as large as -142 mV, compared with the reference sample (without both Y_2O_3 and Al_2O_3). In addition, a group of six cycles Al_2O_3 and with two cycles Y_2O_3 can neutralize the V_{FB} shift to as small as $+3$ mV, which means dipole moments formed at the intermixed high-k dielectric interfaces can neutralize each other to weaken dipole strengths in the wholescale. This phenomenon can be explained by the amorphous properties of the ALD-growth material [22]. Due to the intermixed growth, $Al_xY_{2-x}O_3$ is most likely formed at the interface between $HfO_2$and SiO_x, which is inferred to have a medium oxygen areal density compared to Al_2O_3 and Y_2O_3 based on the experimental observations. As a result, it is possible to find an appropriate combination of dipole layers for specifically desired shifts within the range of millivolt.

Moreover, concise control of threshold voltage is of critical importance to modern very large scale integration (VLSI) design of specific ultralow-V threshold (ULVT), low-V threshold (LVT), standard V threshold (SVT), and high-V threshold (HVT) cells to meet the requirement of both operation speed and power consumption. Si NWFET optimized by IDE can avoid high subthreshold leakage current by enhancing the gate control and maintaining a faster speed at the same time. Large threshold voltage tune can be achieved by either using higher/lower oxygen areal density dielectrics such as SrO or La_2O_3 [10] or increasing the repetition number of the as-design superstructure stack (Y_2O_3/SiO_2 or Al_2O_3/SiO_2) in the gate-stack since the dipole moments can remain within the superstructure [9]. However, the tradeoff between EOT and V_{TH} shift should be carefully taken into consideration in this case.

IV. Conclusion

In summary, the dipole effect of sub-1 nm ALD $Al_2O_3$and $Y_2O_3$is investigated on V_{FB} of MOS capacitors and V_{TH} shifts in n- and p-SOI planar/NWFETs. The results indicate a bidirectional V_{TH} shift can be realized by inserting dipole layers between the SiO_x and HfO_2. More importantly, such shifts were only observed when the dipole layers were deposited in direct contact with SiO_x indicating that the dipole formed at SiO_x/high-k interface is responsible for the phenomenon. Furthermore, intermixed multiple dipole layers in different compositions are also systematically studied here by high-k stacks of HfO_2 and Al_2O_3 and Y_2O_3, to control the V_T shift strengths and directions in a more tailored way. This work deepens the understanding of IDE and provides a feasible design to concisely tune the threshold voltage of MOSFET in a 3-D advanced structure.

Acknowledgment

The authors would like to thank the technical support and guidance of Wei-E. Wang and Mark Rodder from the Advanced Logic Laboratory at Austin of Samsung Semiconductor, Inc.

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